Proposal for US-ATLAS

R&D for a new MDT Chamber Service Module for the ATLAS Phase-II Upgrade of the Muon Spectrometer

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This proposal is to request funding for R&D at the University of Michigan for the Phase II upgrade of a new MDT Chamber Service Module at ATLAS, which must be capable of taking advantage of the increased rates expected at the HL-LHC. The total requested funding for this work is $Xk distributed over three years, from FY2015 to FY2017. We would like to emphasize that critical R&D should be conducted immediately in FY2015 to allow us to make significant contributions to the ATLAS Phase II TDR, scheduled in 2016. This proposal provides a brief introduction, followed by a description of the current MDT readout electronics and the proposed R&D. The budget justification and a timeline for the work is given at the end. For completeness, an estimate of the construction costs for replacing all CSM in the ATLAS muon spectrometer is also included.

1 Introduction

After the Phase II upgrade, planned for 2022, the luminosity will improve to 7×10^{34} cm^{-2}s^{-1} due to further improvements in the accelerator complex, including increased focusing at the interaction region. At this luminosity, the ATLAS experiment is expected to collect 3000 fb^{-1} over 10 years of operation [3]. This will correspond to 85% of the total collision data collected at the ATLAS detector over the lifetime of the experiment. Triggering on high p_T leptons is essential to study many physics processes at this increased luminosity. The current MDT readout electronics have a rate limit of roughly 100 kHz/tube. However, internal ATLAS studies indicate that at Phase-II luminosities the average tube hit rate will exceed 100kHz in the barrel, 60kHz in the outer wheel and 150kHz in the big wheels, requiring the replacement of current MDT readout electronics for almost the entire ATLAS precision muon system. The rate will be reduced by the addition of Level-0 MDT information to Level-1, which will sharpen the p_T threshold on the muon trigger - mitigating the extremely large cross section for muons with $p_T < 20$ GeV/c mis-measured above threshold, see Figure 1. The target design parameters for the ATLAS Phase-II detector electronics are a maximum Level-0 rate of 1 MHz with a minimum latency of 6 μs but required to be designed for at least 10 μs, and a maximum Level-1 rate of 400 kHz with a minimum latency of 30 μs but required to be designed for at least 60 μs. Additionally, the electronics must be able to trigger on successive beam crossings at both Level-0 and level-1.

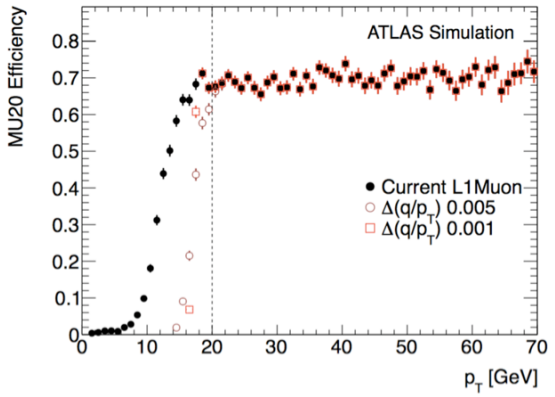

Figure 1: Simulated efficiency of the high p_T muon trigger ($p_T > 20$ GeV/c) with current and upgraded spectrometer p_T resolution.

The two largest components to the upgrade of the MDT readout electronics are the replacement of the mezzanine card, containing three amplifier shaper discriminators (ASD) and a time digital converter (TDC), and the chamber service module (CSM). The mezzanine card is responsible for charge sampling and time-stamping signals from the MDT. The CSM broadcasts timing and control signals to the mezzanine card, and collects data from the mezzanine for readout in response to a Level-1 trigger. The University of Michigan (UM) is the sole institution responsible for the current CSM, and R&D towards its upgrade for Phase-

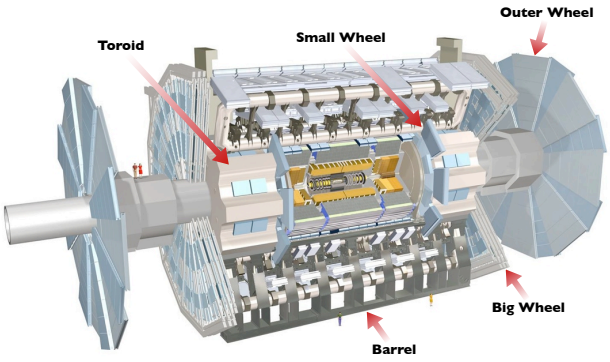

Figure 2: The ATLAS muon spectrometer consists of a central tracking region, the barrel, which covers the region $|\eta| < 1.0$, and the end-cap system which covers the $1.0 < |\eta| < 2.4$ for triggering and $1.0 < |\eta| < 2.7$ tracking. Precision measurement of muon momentum is performed, in almost all the spectrometer, by the Monitored Drift Tubes (MDTs).

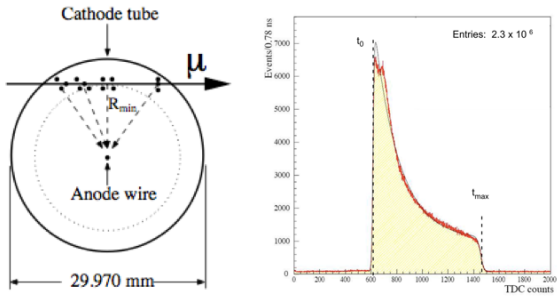

Figure 3: (LEFT) Cross-section of an MDT tube with ionized charge along a track. (RIGHT) Drift time spectrum.

II. UM designed, fabricated, and tested the existing chamber service module (CSM) of the MDT readout electronics, and continues to maintain all CSM modules currently used. We are currently in discussions with US-ATLAS to take on the construction of all CSM boards required by the ATLAS muon spectrometer ($\sim$1300 boards). UM's cost estimates have been very well received by US ATLAS management (included in this proposal), which have been informed by our previous experience in the design and construction of the current CSM boards in operation at ATLAS. UM was also primary in the overall MDT installation, commissioning, and maintenance. The Phase II upgrade of the MDT readout electronics, in particular the CSM, will be a primary focus of UM R&D over the next three years and beyond. The Phase I and II upgrade of the LHC experiments "constitute the highest-priority near-term large project" (Recommendation 10) according to the strategic plan for US particle physics developed by the P5 committee in 2014 [1]. Further, US-ATLAS considers the upgrade of the CSM, UM's primary Phase II deliverable, as the highest priority component of the Phase II upgrade of the ATLAS muon system, "Under the assumption of reduced budget we will assign highest priority to the CSM development" by US-ATLAS management [2].

2 MDT Precision Tracker and Current Readout Electronics

The monitored drift tube (MDT) chambers are the primary component of the precision muon tracking system, shown in Figure 2 [5]. The precisely manufactured MDT chambers are carefully monitored within the ATLAS detector for their position, internal deformations, and environmental conditions like temperature and magnetic field. Due to the combination of mechanical accuracy of each chamber and external position monitoring (alignment), the MDT system achieves a sagitta accuracy of 60 μm, corresponding to a momentum resolution of about 10% at p_T = 1 TeV/c. The 1,150 MDT chambers, of various sizes and geometries, are made from 354,000 tubes and cover an area of 5,500 m^2. The cross-section of an MDT tube is shown on the left in Figure 3. The MDT are pressured gas (3 bar of 93%Ar, 3%CO_2) drift tubes with a diameter of 30 mm, operating at about 3 kV. Electrons are ionized in the gas along a charged particle track (gas gain = 2×10^4), and drift radially towards the central wire of the tube. The drift velocity of an ionized electron has a strong dependence on the radial distance from the central wire, ranging from 10 μm/ns close to the outer

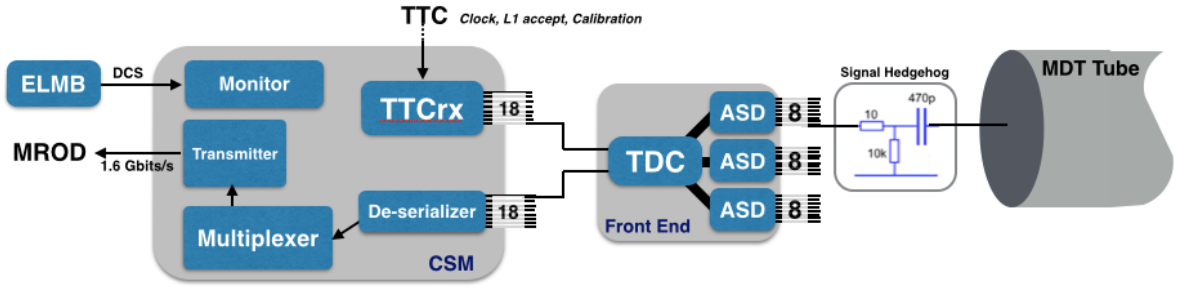

Figure 4: Block diagram of the current MDT front-end electronics.

wall to 50 μm/ns close to the wire. Each track will produce a similar radius-to-drift time shape (r-t relation), where the start and stop time correspond to the minimum radial distance of the track and the outer radius of the tube, respectively. On the right of Figure 3 displays an example of the drift time spectrum for tubes in a middle barrel chamber. With the r-t relation understood to high accuracy, precision measurements of the track distance from the center of the tube can be extracted. The average spatial resolution is 80 μm for an MDT tube and 40 μm for an entire chamber.

The architecture of the MDT readout system is shown in Figure 4, a photograph in Figure 6, and a detailed description is given in [6]. The main task of the readout electronics is to preserve the measurement accuracy of the MDT tubes, and to handle the high hit rates at LHC luminosities. The signal and high voltage electronics for the tubes are isolated from each other by two so-called hedgehog boards, which are simply RF decouplers. The raw drift signals for up to 24 tubes are amplified, shaped and digitized by three ASD chips, and then routed to a Time-to-Digital Converter (TDC) on a front-end board. A block diagram of the TDC is shown in Figure 5. The TDC stores the arrival times of the leading and trailing edges of the signal, as well as an identifier word for the corresponding tube, in a buffer memory of 256 words. These times are measured in units of the Timing, Trigger and Control (TTC) clock, which operates at the bunch crossing frequency of the LHC (40.08 MHz). Timing for triggered hits are matched to corresponding bunches and passed to a readout FIFO to be sent to the Chamber Service Module (CSM). Up to 24 tubes can be served by a single front-end board, which contains three ASD chips and a TDC chip. One MDT chamber can have up to 18 front-end boards. The CSM, shown in Figure 7, broadcasts the TTC signals to the TDCs, and collects data from the TDCs in response to a Level-1 trigger. At the CSM, the data are formatted, stored in a large de-randomizing buffer, and sent via

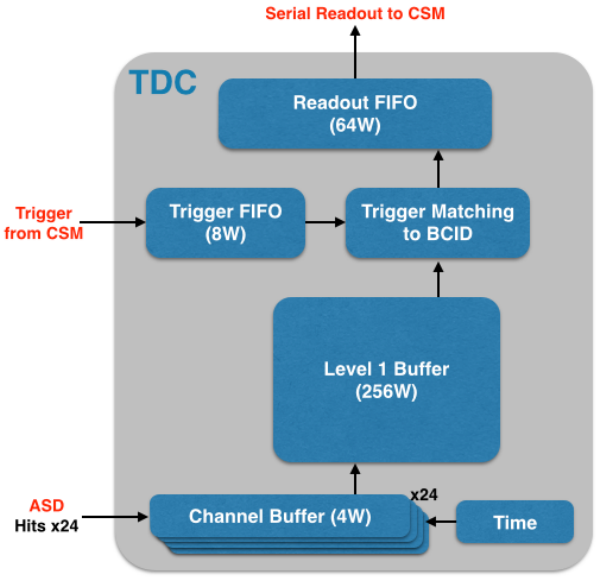

Figure 5: Block diagram of the current Time-to-Digital Converter (TDC) on a front-end board. The TDC stores the arrival times of the leading and trailing edges of the signal, and on a Level-1 trigger, sends this data to the CSM for readout.

optical link to the MDT readout driver modules (MROD). The CSM communicates with the off-chamber electronics via two fibers, one coming from the TTC distribution box and the other going to the MROD. The MROD is a VME module, serving up to six CSMs. The MROD assembles the data associated with each event and transfers it to the Readout Buffer (ROB), where data are stored until the event is either accepted or rejected by the Level-2 trigger. The MROD is also able to monitor incoming data and search for deviations from nominal values which could be evidence of a malfunction.

Initialization of the CSM and front-end boards is provided through JTAG from an external-local-monitor-board (ELMB). The ELMB interfaces to the CSM via optic couplers. Detector control, monitoring, and JTAG are all received by the ELMB from data sent on a CANbus. In addition to reading out the MDT chambers, electronics on the CSM and front-end boards monitor the chamber environment and running conditions and supply low and high voltage power. The total power consumption of a single front-end board is 1.6 W and for a CSM board is 4 W. High-density 40 pin twisted pair cables are used to transmit control signals as well as supply power for front-end and CSM boards.

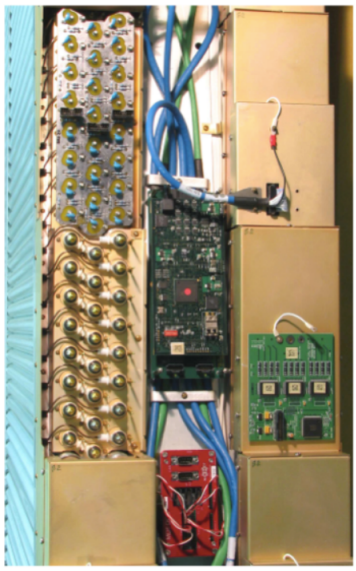

Figure 6: Readout end of an MDT chamber. Hedgehog boards are attached to the tube ends (left). A mezzanine board (right), CSM (center), and ELMB (bottom) are also visible.

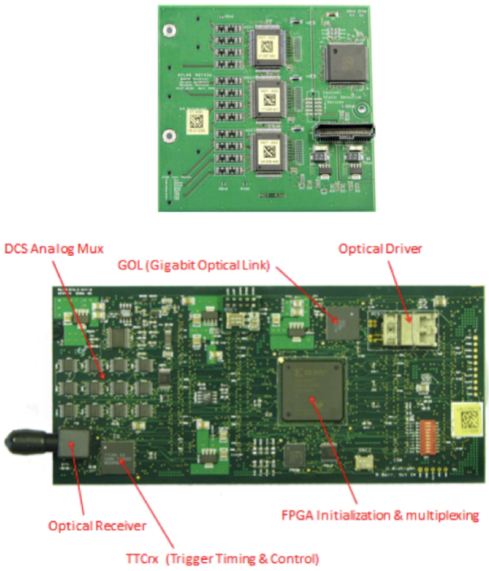

Figure 7: (Top) front-end or mezzanine board, which includes three ASD chips and one TDC chip. (Bottom) Chamber Service Module (CSM).

3 R&D for the ATLAS Phase-II MDT Front-End Electronics

A large team at UM will conduct R&D for Phase-II, led by Tom Schwarz, together with faculty Amidei, Chapman, Qian, Zhou, Zhu, research staff Ball, Dai, and Levin, and excellent engineers Liang Guan, Xueye Hu, Jinghong Wang, as well as several engineering students. However, the budget request for this proposal is to support only X. All other contributions come from the UM DOE base program.

The target design parameters for the ATLAS Phase-II detector electronics are a maximum Level-0 rate of 1 MHz with a minimum latency of 6 μs but required to be designed for at least 10 μs, and a maximum

Level-1 rate of 400 kHz with a minimum latency of 30 μs but required to be designed for at least 60 μs. In addition, the electronics must be able to trigger on successive beam crossings at both Level-0 and Level-1. R&D at UM is divided into several work streams towards accommodating these requirements in a design of a new CSM for the Phase-II Upgrade of the Muon Spectrometer. These include:

- Development of an accurate simulation of the MDT chamber hit rate expected for the HL-LHC. The simulation will inform design and optimization of both the new front-end electronics, as well as the chamber service module. Further, the simulation will be used to predict whether the current MDT readout in the inner barrel, which are not easily replaced, can cope with the higher rates. An AMT3 VERILOG simulation program will also be modified to use the generated MDT hits from the simulation for testing the current MDT readout in the inner barrel at HL-LHC luminosities.

- The new readout system will require increased bandwidth from the mezzanine TDCs to the CSM and from the CSM to trigger processing, and additional buffering at both the mezzanine and CSM. Hit rates from simulation will be translated into required bandwidth (bit rates) and buffering (memory) for candidate designs to meet Phase-II triggering specifications by our engineers.

- The Timing, Trigger and Control (TTC) and Monitoring functions performed by the TTCrx and Embedded Local Monitoring Board will be replaced by CERN GigaBit Transceiver (GBT) components, including a high-speed bi-directional radiation hard optical link (GBTx) and an interface to slow-controls (GBT-SCA). The GBT will require a separate board to handle multiple CSMs. R&D will be carried out necessary to understand the GBT chipset and incorporate it into the design of the CSM.

- Current CSM boards are connected to the mezzanine boards through a motherboard, which essentially serves to handle the large number of cables from the front-end and re-route them to more compact pin connectors which connect to the CSM. It is not clear whether these cables and motherboards need to be replaced for Phase-II. If so, a great deal of personnel will be required, and will significantly increase construction costs. Research scientist Dan Levin is leading the effort to evaluate the boards/cables for Phase-II rates and develop a solution that hopefully does not require replacement.

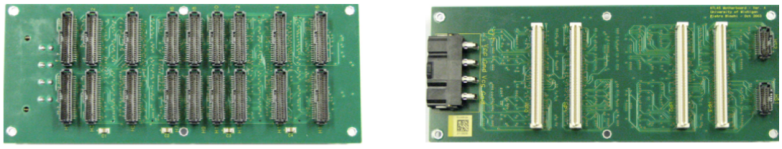

Figure 8: Front and back of the motherboard which serves to connect the many cables from the front-end boards to more compact pin connectors which attach to the CSM.

- The front-end link exchange system (FELIX) will replace the ROD-ROS (readout driver and storage) to perform data collection from the CSM. This is not a significant change for the design of the CSM. However, it may require a change to the CSM output protocol in addition to changing the speed of the links, which must be investigated by our engineers.

- The largest change to the CSM board is the addition of a trigger path for Level-0 MDT information to be passed to the Level-1 trigger algorithms off detector. This is the heart of the Phase-II upgrade for muon electronics. Hu will be developing a scheme for the MDT trigger data selection and format,

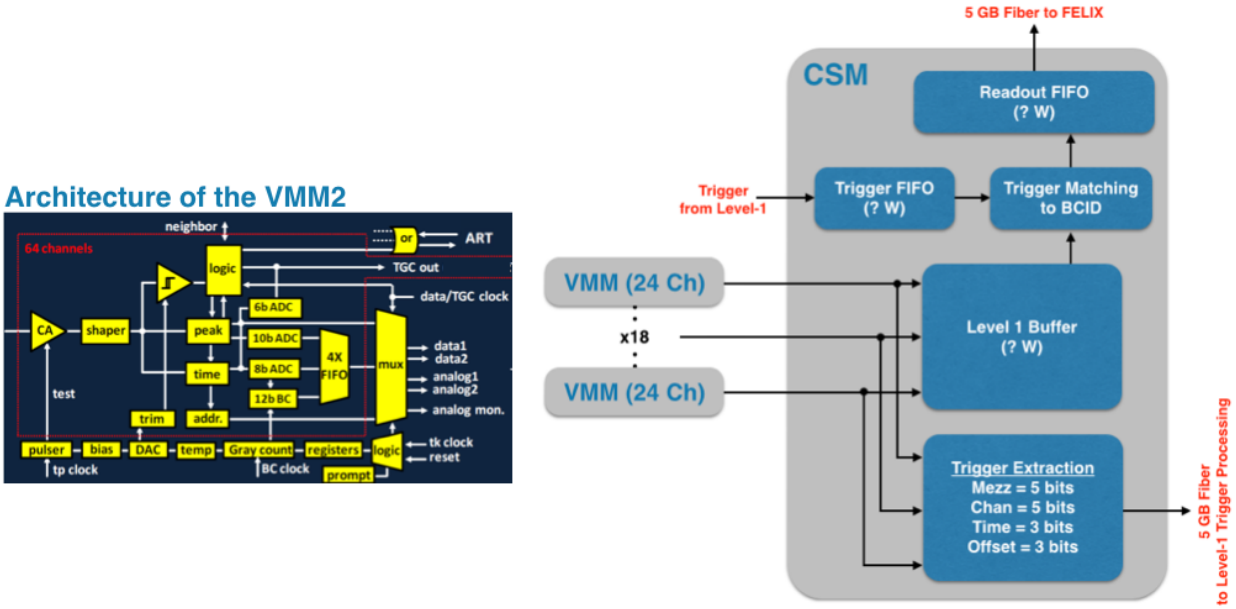

Figure 9: Diagram of a candidate design for the new MDT readout electronics, including the use of the VMM for sampling and time stamping.

including the bandwidth requirement, in collaboration with trigger developers at MPI Munich and KEK .

- The FPGA must function in a higher rate environment and the single bit upset rate should be within acceptable limits. This issue will be investigated in connection with Phase-I research for the router, where radiation tolerance of candidate FPGAs for the NSW router must be understood. Additionally, firmware capable of mitigating the single event upset rate will be designed.

- BI (barrel inner) MDT chambers are not easily accessible and their front-end electronics is not planned to be replaced. Solutions must be investigated by engineers such that new CSM design is compatible with the previous front-end for these chambers.

R&D from these projects will inform prototype design for the new CSM, which must be completed in time to be integrated into the ATLAS Phase II TDR, scheduled for CERN project approval in 2016. Hu will be the primary designer of the CSM board, including programming of the multiplexing algorithm for the FPGA, schematic design of the PCB board, component selection, and layout. A few prototypes will be constructed and accurately evaluated by Hu and our in-house electronics technician Jon Ameel.

Several high-level designs are already in consideration. Figure 9 outlines one such candidate design for the new MDT readout system. A 24 channel ASIC, based on the VMM2 developed for the new small wheel, could be used to perform both the ASD and TDC functionality on the front-end, with Level-1 trigger matching implemented in the CSM. In this system, the new CSM would serve as a buffer for MDT signals to be read out on a Level-1 accept, and would provide reduced resolution hits (Level-0) for Level-1 decisions. Detector control/monitoring and timing tasks are expected to be performed by the newly-developed CERN GBT system. The GBT system will also broadcast timing signals to the front-end through the CSM. This design would utilize existing cables between the motherboard and the mezzanine, and require fiber optic

cables from the CSM to FELIX and to Level-1 trigger processing. With this basic outline of a design we can use predicted HL-LHC MDT hit-rates, extrapolated from 8 TeV data, to estimate needed bandwidth and buffering memory. The Level-1 buffer on the new CSM is required to hold hits before a Level-1 trigger accept. If the highest rate the new front-end will experience is typified by 200 kHz/tube, the Level-1 buffer will experience a 4.8 MHz rate (0.22 hits per mezzanine per bunch crossing). This rate leads to 25% of the bandwidth occupied from the VMM to the CSM and an average 250 slots filled in the Level-1 buffer during the 60 μs latency. Assuming a 400 MHz Level-1 accept rate, 22% of the bandwidth will be occupied from the CSM, off-detector, to processing at USA-15. Modern FPGA's are well-capable of handling these rates and memory requirements, therefore as a first pass this is encouraging for this design. The R&D outline in this proposal will be used to further understand the expected performance and costs for multiple candidate designs, culminating in a design choice for the ATLAS Phase-II TDR.

3.1 Requested Support and Timeline for R&D

The total proposed funding for this R&D is $Xk distributed over three years, from FY2015 to FY 2017, detailed in Figure 10 below. These funds will be used to support X. DESCRIPTION OF ACTIVITIES OF PERSONNEL.

In addition to personnel, some modest support is requested for travel, materials and supplies. Radiation testing for candidate components will begin in FY2015. Based on previous experience for the current CSM and for the Phase-I upgrade, radiation testing will take roughly 8 hours per exposure at a cost of roughly $1k/hour. Funding for domestic travel is also required to bring personnel to the testing site, and possibly to potential part manufacturers. In addition, we anticipate roughly one trip per year to CERN for our engineer for workshops and collaboration with other members of the ATLAS Phase-II upgrade effort. Other members of the UM group contributing to the Phase II effort, namely Amidei, Dai, Levin, Neal, Qian, Schwarz, Zhou, Zhu as well as several graduate students and postdocs, are supported by the DOE base grant at UM.

The timeline in Figure 11 summarize R&D activities and milestones. Initial R&D, beginning in FY2015, will be defining the specifications of the CSM board at high luminosity with MC simulations, investigating the suitability of current front-end to CSM motherboards/cables, and understanding FPGA radiation requirements and commercial chip tolerances and gaining familiarity with the GBT system. In FY2016, development of FPGA firmware such as the multiplexer and new Level-0 trigger path, and design selection will be performed. Initial prototypes and test fixtures will be constructed for component evaluation and testing designs. The selected design will be included in the Phase II ATLAS TDR, scheduled for project approval in 2016. This will be a significant contribution to the TDR by UM. In FY2017, refinement of the design and additional prototyping will be conducted. Construction for the Phase-II upgrade of the CSM will begin in FY2018.

Figure 10: Requested personnel/funding to support R&D for the Phase-II MDT readout electronics. Total requested funding is $Xk for FY15-FY17

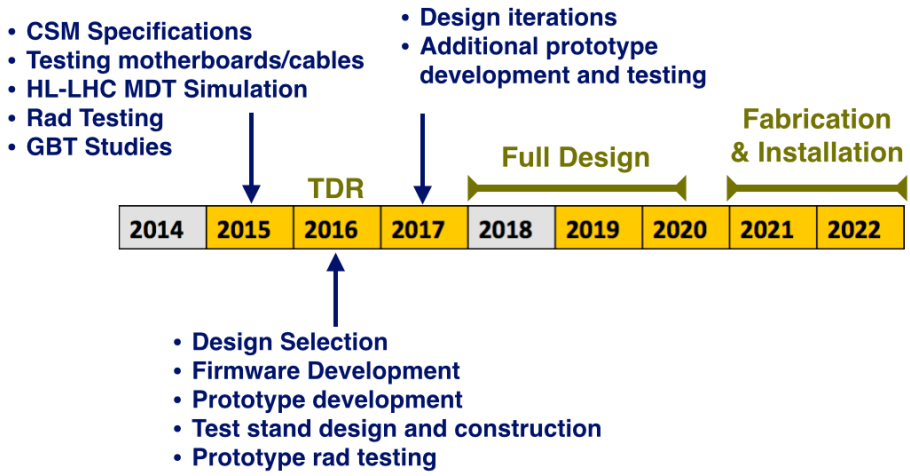

Figure 11: Summary of Phase-II MDT electronics R&D activities and milestones.

3.2 Estimated Construction Costs for the CSM Upgrade

Though this proposal concerns the work and costs associated with the necessary R&D to define the construction of the Phase-II CSM boards, it is worth documenting current estimated costs for the construction phase of the upgrade. The total number of CSM boards can be calculated from the current number of boards, taking into account a few new chambers and the Phase-I new small wheel, which will not need upgraded CSM. There are currently 624 chambers in the barrel and 546 in the end cap, which require 608 and 510 CSM boards, respectively. The NSW will not require CSM, so subtract 64 CSM. There are several new chambers, including the BME/BMR, BOE/BOR, BMG, which will require 22 additional CSM. We will assume an 85% yield and the need for 10% spares. With a few additional nuances, the number of CSM boards required for Phase-II will be 1325.

To estimate fabrication costs, we use the baseline design previously mentioned, including new FPGAs and replacing the TTCrx, GOL, lb42, and slow control with the GBT system and similar costs to the current ATLAS CSMs, accounting for new components, inflation, and exchange rates [9]. Costs for new components are either taken from recent listed costs or from estimates of the developer/manufacturer. Fabrication, assembly and shipping costs per board are estimated from previous costs adjusted for inflation. We applied inflation rates, 0.26 measured from 2003-2014, and 0.03 from 2014 to 2021. Exchange rates were taken as 0.74 USD/CHF in 2003 and 1.14 USD/CHF in 2014. Detailed breakdown of the construction costs estimated for the Phase-II CSM boards are shown in Figure 12.

Predicted personnel for construction of the Phase-II CSM is also taken from previous experience. Development of the current CSM boards was led by a Senior Engineer at UM (Jay Chapman). Jay also led the firmware design of the CSM FPGA. Roughly the effort equivalent of two engineers at UM (Pietro Binchi, Bob Ball, Tiesheng Dai, and Jon Ameel) performed board design, CSM firmware, test fixture design, debugging, and production. Two engineering students assisted with some development and testing and debugging. Based on these previous resources, we have put together expected personnel and associated costs, shown in Figure 13. The total construction costs are equivalent to those in 2003, accounting for inflation, exchange rates, and the number of proposed fabricated boards. Note in 2003, collaborators in Israel covered the costs of construction for nearly half of the CSM boards. This was a unique agreement, and not expected to be duplicated for Phase-II.

Components	Count	Cost / item	Total Cost	Basis of Estimate
FPGA's	1325	$279.323	$370,103	201-05
PROM's	1325	$15.802	$20,938	201-05
Optoelectronics (2 per board)	2650	$105.154	$278,658	Phase-I
GBT-SCA	1325	$33.649	$44,585	CERN
Misc Parts	1325	$175.015	$231,895	201-05
Fabrication and Assembly		$157.400	$208,555	201-05
Total Cost		$766	$1,154,734	

Figure 12: Estimated fabrication costs for a single CSM board, including new FPGAs and slow control with the GBT system. Other components were estimated from similar costs to the current ATLAS CSMs, accounting for inflation and exchange rates. [9]

References

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		FY18		FY19		FY20		FY21	
		%	$ / hr	%	$ / hr	%	$ / hr	%	$ / hr
Personnel Effort and $/hr	Sr. Engineer	0.5	$93.48	1.0	$96.28	1.0	$99.17	1.0	$102.15
	Jr. Engineer	0.5	$57.90	1.0	$59.64	1.0	$61.43	1.0	$63.27
	Elec. Technician	0.5	$56.85	1.0	$58.56	1.0	$60.31	1.0	$62.12
	Elec. Student	0.5	$35.48	1.0	$36.54	1.0	$37.64	1.0	$38.77
Costs	Total Personnel Cost		$216,414		$445,814		$459,188		$472,964
	Travel		$8,000		$8,000		$8,000		$8,000
	Prototypes/Fixtures/Software				$35,000		$20,000		
	Final Production								$1,154,734
	Shipping								$35,000
	Total Cost		$224,414		$488,814		$487,188		$1,670,698
								Total	$2,871,114

Figure 13: Estimated total costs for the construction of all Phase-II MDT CSM boards, including expected personnel and fabrication. Personnel and fabrication costs are based on those required for the current CSM boards, or quotes from developers/manufacturers.